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OPTICAL INTERCONNECT IN FUTURE SYSTEMS ON CHIP

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ABSTRACT: The shift to very high performance distributed Multi-Processor Systems-on-Chip (MPSoC) as mainstream computing devices is the recognized route to address, in particular, power issues by reducing individual processor frequency while retaining the same overall computing power. However, the move to such architectures requires organized high-speed communication between processors and therefore has an impact on the interconnect structure. It clearly relies upon the existence of an extremely fast and flexible interconnect architecture, to such a point that the management of communication between processors will become key to successful development. Optical interconnects and optical network on chip (ONoC) architectures are emerging as potential contenders to solve congestion and latency issues in future computing architectures. In this tutorial, I will firstly present the constituent elements of a basic integrated optical interconnect link and associated technology and design issues. I will then cover quantitative comparisons for direct point-to-point links, using single-wavelength links instead of electrical links, and will finally describe the architecture of an optical network on chip, exploiting wavelength routing to achieve specific network connectivity requirements.

BIOGRAPHY: Sébastien Le Beux is Associate Professor for Heterogeneous and Nanoelectronics Systems Design at Ecole Centrale de Lyon since 2010. In 2013, he is invited scholar for 6 months in the Department of Electronic and Computer Engineering from the Hong Kong University of Science & Technology. From 2008 to 2010, he was postdoctoral researcher at Ecole Polytechnique de Montréal (Computer and Software Engineering department), Canada. In 2007, he obtained a PhD in computer science (INRIA grant). Relying on significant expertise from previous projects in both modelling and design methods for emerging (nano)technologies and embedded systems, the research interests of Sébastien Le Beux cover Optical Network on Chip, design space exploration, design methods and dynamic reconfiguration. Sébastien Le Beux has 6 articles published in refereed publications (journals), 3 book chapters, 7 invited and over 20 regular articles published in refereed international conference proceedings (1 recipient of Best Paper Award, NEWCAS 2011), over 30 talks in conference/workshop and 1 patent. He is the organizer of the ISCAS 2013 special session on silicon photonic architectures, the program chair of FETCH 2011, 2012 and 2014 (French winter school on heterogeneous system design) and the co-chair of the DATE session on Embedded Software for Many-Core Architectures in 2013 and 2014. He is TPC member of DATE (since 2012), GLSVLSI (since 2011), NANOARCH (since 2012) international conferences and regular reviewer for IEEE TVLSI, IEEE TCAD, IEEE TPDS and Elsevier JSA journals.